Electrical Effects of a Single Extended Defect in MOSFETs

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***Abstract*— The electrostatic and leakage effects of extended defects on Si and Ge MOSFETs are investigated. A technology computer-aided design model of extended defects is developed based upon measured device electrical properties. A single extended defect is introduced into simulated 2-D planar and 3-D FinFET structures. It is found that a 2-D extended defect is a source of variability in planar transistors, with the electrical effects depending on its position along the channel. A 2-D extended defect increases the threshold voltage and subthreshold swing when it is in the channel and increases the leakage current when it is in the drain. The dislocation effect on transistor characteristics increases with decreasing transistor width. The effect is less pronounced in FinFETs due to the well-controlled electrostatics and the small dislocation volume.**

***Index Terms*— Dislocation, extended defect, FinFET, germanium, MOSFETs, technology computer-aided design.**

I. Introduction

ONE of the concerns with respect to the integration of high-mobility channel materials on silicon is the presence of extended defects, due to the lattice and thermal mismatch with the substrate [1]. Above a certain epi-layer thickness, the strain will relax by the formation of misfit and threading dislocations (TDs) [2]. The main concern is the associated electrical activity, which can dramatically affect the device performance [3]–[7]. This leads to efforts spent in reducing the defect density during epitaxial growth by employing optimized strain-relaxed buffer layers for the fabrication of Ge or III–V virtual substrates on silicon [8], [9]. Alternatively, in a shallow trench isolation (STI) first approach, the top layer of a Ge or III–V fin can be grown defect-free by the aspect-ratio-trapping effect, where the inclined TDs are trapped by the SiO_2 sidewalls for a sufficiently large aspect ratio (depth/width > 3) [10]. However, as shown recently, this only holds for the smallest dimension, while along the trench direction (transistor width), new extended defects can be nucleated, which penetrate the surface of the fin [11], [12]. When scaling down the transistor dimensions further, the probability of finding a dislocation (or other type of extended defect) may become small, so it becomes a variability issue more than a degradation issue. 1-D or 2-D extended defects (stacking faults, twins, and so on.) can be introduced in bulk FinFETs by certain processing steps, such as ion implantation and annealing [13], by the application of a silicon passivation step for Ge pMOSFETs [14] or the selective epitaxial growth of highly doped (and strained) source/drain regions [15]. Thus, there is always a finite probability that a single nanoscale transistor contains an extended defect.

It is well-known that dislocations (e.g., in germanium) exhibit electrical activity [2], [16]. This has been evaluated for the case of Ge virtual substrates on silicon by measuring the diode leakage [3]–[6] and/or the impact on Hall mobility and resistivity [7]. The same can be applied to wide selective Ge deposition between STI [17], [18]. In that case, rather large junction structures are typically used, containing several thousands of dislocations and yielding an average leakage current per TD or, equivalently, a generation or recombination lifetime per dislocation. For bulk FinFETs, on the other hand, it is less obvious how to translate these results obtained on macroscopic devices to nanometric volume Ge or III–V regions containing only one or a few extended defects.

One question that arises concerns the role of the relative position of a dislocation with respect to the source, drain, or channel. It has been shown that this is an important issue with respect to stacking faults in silicon-on-insulator (SOI) MOSFETs [19], [20]. Given the small volume of the fins, experimental assessment of the electrical activity of extended defects becomes problematic and requires more sophisticated analysis techniques than simple current–voltage (I–V) measurements on relatively large diodes or Hall effect measurements. In general, structural and electrical characterization has to be performed simultaneously in order to detect the presence of a defect, e.g., relying on scanning probe techniques [21]. This brings technology computer-aided design into the picture, where it is possible to predict qualitatively, and when properly implemented and calibrated, also quantitatively the effect of a single extended defect on the performance of FinFETs. It also allows numerical experiments to be performed to quantify the effect of relative defect position on the resulting parametric variability.

This paper examines the electrical impact of a single dislocation in a nanoscale transistor through simulations based

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TABLE I
PARAMETERS FOR DISLOCATION

Symbol	Quantity	Value	Ref.
$\boldsymbol{b}$	Burgers vector	$\frac{1}{2}<1\bar{1}0>$	[2]
α	Angle between the dislocation line and the Burgers vector	60°	[2]
f_{dis}	Occupation of dislocation	10%	[16]
r_{dis}	Radius of the dislocation	2 nm	[2]
σ	Capture cross section of traps inside dislocation	$3\text{x}10^{-13}$ cm^{-2}	[4]
υ_{thn}	Electron thermal velocity	$2.5\text{x}10^{7}$ cm/s	[26]
υ_{thp}	Hole thermal velocity	$1.6\text{x}10^{7}$ cm/s	[26]
τ_{dis}	Carrier lifetime inside the dislocation	$1/N_{dis}\upsilon_{th}\sigma$	[25]

on experimental observations. The dislocation is considered as a cylindrical arrangement of midgap acceptor states with a density N_{dis} and radius r_{dis} [22]. Shockley–Read–Hall (SRH) generation–recombination models are applied for these acceptor states. The dislocation parameters chosen for simulation are validated by experimental data from the literature. Section II provides the physical model and details on how the model parameters are validated by measured data. In Section III, the proposed model is applied to different kinds of MOSFETs.

II. SIMULATION METHOD

To study the electrical impact of a single dislocation in a transistor, the midgap acceptor trap density N_{dis} and carrier lifetime τ inside the dislocation have to be estimated. It is known that the line density of acceptor states along the dislocation is given by [22]–[24]

$$N_{\text{line}} = \frac{1}{c \cdot f_{\text{dis}}} = \frac{\sin\alpha}{0.866b \cdot f_{\text{dis}}} \tag{1}$$

where N_{line} is the line density of the acceptor states and c is the distance between acceptor states along the dislocation. The other parameters are listed in Table I. From the line density and the cross-sectional area of the dislocation, the volumetric trap density inside a dislocation is given by

$$N_{\text{dis}} = \frac{N_{\text{line}}}{\pi r_{\text{dis}}^2}. \tag{2}$$

With the parameters in Table I, based on the values in the references, the trap density is estimated to be $N_{\text{dis}} \approx 10^{19}$ cm^{-3}.

The lifetime τ_{dis} inside a dislocation is given by SRH theory

$$\tau_{\text{dis}} = \frac{1}{N_{\text{dis}}\upsilon_{\text{th}}\sigma}. \tag{3}$$

With the values chosen as shown in Table I, the lifetime inside a dislocation is estimated to be $\tau_{\text{dis}} \approx 10^{-14}$ s.

This value can also be confirmed from measured data of the generation lifetime τ_g on p-n junctions [25]. The measured generation lifetime τ_g is a macroscopic lifetime in the sense that it includes contributions from both the defective and nondefective areas. To get the lifetime inside the dislocation, proper scaling is needed. In this paper, a simple scaling theory is considered. The generation leakage current density J inside a p-n junction with depletion width W is given by

$$J = \frac{qWn_i}{\tau_n}(1 - A_{\text{dis}} \cdot \text{TDD}) + \frac{qWn_i}{\tau_{\text{dis}}}A_{\text{dis}} \cdot \text{TDD} \tag{4}$$

where n_i is the intrinsic carrier density, τ_n is the carrier lifetime in the nondefective area, A_{dis} is the cross-sectional area of a single dislocation, and TDD is the TD area density. The first term is the leakage current density from the normal nondefective region weighted by the area, while the second term is the leakage current density from the dislocation. In the case where the leakage current is dominated by dislocation-induced leakage, the lifetime in the dislocation is

$$\tau_{\text{dis}} = \frac{A_{\text{dis}}}{\frac{1}{\tau_g}/\text{TDD}} \tag{5}$$

where τ_g is the measured generation lifetime, which is inversely proportional to the TD density TDD [25]. Based on experimental data, this lifetime is estimated to be $\tau_{dis} \approx 4.6 \times 10^{-14}$ s. This value is close to that estimated from SRH theory, confirming that the SRH approach is consistent with experimental values.

III. SIMULATIONS AND DISCUSSION

A. 2-D Si nMOSFET

With the dislocation parameters, namely, trap density, carrier lifetime, and orientation defined, the dislocation is introduced into a 2-D Si nMOS device, including the SRH, trap-assisted tunneling (TAT), and band-to-band tunneling models provided by [27]. The simulated device has a gate length $L_G = 30$ nm and effective oxide thickness EOT $= 1$ nm. To study the possible variability related to the relative dislocation position, the dislocation is shifted in 20-nm steps from the source side to the drain side. Fig. 1 shows three such steps, where step 3 is in the source side, step 5 intersects the channel, and step 9 is in the drain side. Fig. 1 also shows the trapped electrons in the device when biased at $V_G = 1$ V, $V_D = 50$ mV, and $V_S = V_B = 0$ V. It is clear that the degenerate source/drain n-type doping and the inversion charge in the channel keep the midgap acceptor traps occupied and consequently negatively charged. This is because the electron quasi-Fermi level is close to the conduction band, above the midgap level in all three cases. Similarly, the traps inside the dislocation are largely empty when they are inside the substrate, which has over 10^{17} cm^{-3} p-type doping.

Fig. 2(a) shows the substrate current variation with the dislocation placed at different positions throughout the device, again biased at $V_D = 50$ mV. The source to drain leakage current due to short channel effects is large enough to mask the dislocation-induced leakage current. However, the substrate current in the OFF state is dominated by the dislocation-induced leakage current. When the dislocation is in the source side, the substrate current is the same as the no-trap condition, but when the dislocation moves to the channel and further to the drain side, the leakage current increases by approximately three orders of magnitude. This indicates that the additional SRH or TAT leakage generated by a dislocation has a significant effect on substrate leakage, as soon as the dislocation

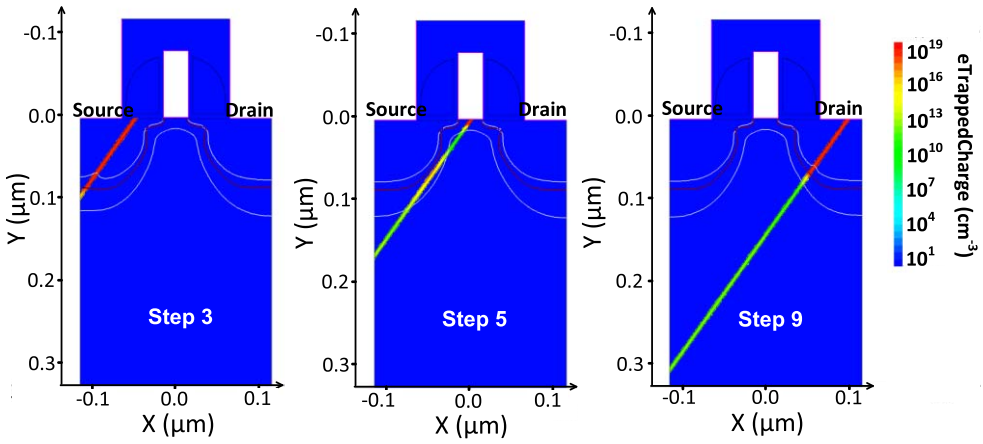

Fig. 1. Trapped electrons inside the device as the dislocation moves from source to drain at $V_G = 1$ V, $V_D = 50$ mV, and $V_S = V_B = 0$ V. The dislocation moves 20 nm each step from source side to drain side. White lines: depletion region boundaries in the device.

crosses from the substrate into the positively biased drain. A similar trend has been measured for the OFF-state current of planar SOI transistors containing a stacking fault at different positions in the channel [19], [20].

Fig. 2(b) shows the transfer characteristic of the transistor with the dislocation placed throughout the device. The device characteristic remains the same as the no-dislocation case when the dislocation is in the source or drain side. The transfer characteristic is affected only when the dislocation intersects the channel. The threshold voltage and subthreshold swing (SS) are increased compared with the no-dislocation case. This is because some of the electrons in the channel are trapped in the dislocation so that a higher gate voltage needs to be applied to reach the same current level. Fig. 2(c) shows the linear and saturation threshold voltage and SS as a function of the dislocation position with $V_D = 50$ mV and $V_D = 0.5$ V. The threshold voltage increases by 70 mV when the dislocation intersects the channel, as compared with when it is located in the source/drain. This indicates that the device characteristic is highly dependent on the dislocation position, which could potentially be a source of static parameter variability.

B. 2-D Si pMOSFET

The 2-D Si pMOSFET doping profiles are the same as those of the nMOSFET, with opposite polarity. The gate work function is adjusted to get a reasonable threshold voltage. The occupation of midgap acceptor traps in the pMOSFET is opposite to that of the nMOSFET. For example, traps in the channel region change from being occupied to empty when the device switches from OFF to ON in the pMOSFET. Traps in the source/drain regions with degenerate p-type doping are empty, while traps in the substrate are filled and become negatively charged. These negatively charged traps create a space charge cylinder around the dislocation in the substrate [2].

The substrate current variation with the dislocation position in the pMOSFET is similar to that in the nMOSFET shown in Fig. 2(a). The substrate current in the OFF state with a dislocation in the drain side is orders of magnitude higher than if it is located in the source side. The pMOSFET has a similar dislocation position dependence as the nMOSFET, as shown in Fig. 3. With the dislocation placed in the source side or drain side, the transfer characteristic is almost the same as for the no-dislocation case. However, when the dislocation is in the channel, the transistor threshold voltage and SS both increase. It shows that the threshold voltage increases by more than 30 mV.

The threshold voltage increases because the negative charge in the dislocation compensates the positive space charge. This reduces the effective density of positive space charge, which leads to an increase in threshold voltage. Since the occupancy of traps in the channel changes when the device turns from OFF to ON, the SS increases. Thus, a dislocation in a pMOSFET has effects very similar to those in an nMOSFET.

C. 2-D Ge pMOSFET

Since Ge pMOSFETs are considered to be promising candidates for further CMOS scaling, it is important to examine the dislocation effects on transistor performance. The simulation setup is the same as the Si pMOSFET, but the material changes from Si to Ge. Since Ge has a lower bandgap compared with Si, much higher leakage can be expected [28]–[30].

Fig. 4(a) compares the substrate current in Ge and Si pMOSFETs with a dislocation at step 3 (in the source side) and step 9 (in the drain side). The substrate current in the OFF state with a dislocation in the drain side is about three orders of magnitude higher than when it is located in the source side in both Si and Ge pMOSFETs. Moreover, the substrate current in the Ge pMOSFET is three orders of magnitude higher than that of the Si pMOSFET in the OFF state, irrespective of the dislocation position. This is consistent with the three orders of magnitude higher intrinsic carrier density in Ge compared with Si [25]. Higher intrinsic carrier density leads to higher leakage current, as illustrated in (4). Moreover, the substrate current in the Ge pMOSFET is almost gate-bias independent when the dislocation is located on the drain side, indicating that the dislocation-induced leakage dominates the substrate current.

Fig. 4(b) shows the device transfer characteristic with the dislocation at different positions. As in the Si pMOSFET case,

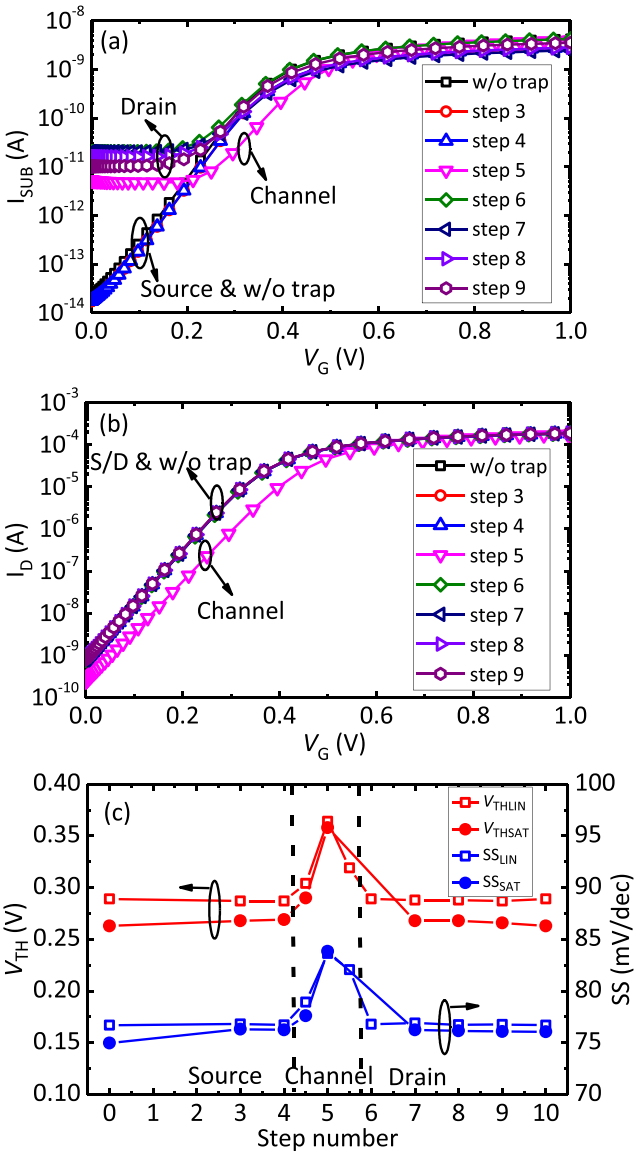

Fig. 2. Si nMOSFET (a) substrate current and (b) drain current as a function of gate bias with the dislocation at different positions inside the transistor at $V_D = 50$ mV. (c) The linear and saturation threshold voltage and SS as a function of dislocation position inside the device with $V_D = 50$ mV and $V_D = 0.5$ V. The region between the dashed lines is when dislocation intersects the channel. Here, step 0 corresponds to the no dislocation case.

the device with a dislocation on the source side has the same characteristic as the no-dislocation case. In addition, only when the dislocation intersects the channel does the threshold voltage and the SS increase. The threshold voltage increases by 35 mV when the dislocation intersects the channel, as compared with other positions. However, the characteristic of a device with a dislocation on the drain side differs from a Si pMOSFET. The drain leakage current increases by three orders of magnitude, as compared with the case when the dislocation is on the source side, as shown in Fig. 4(b). This leakage current comes from the drain to bulk junction leakage, as also shown in Fig. 4(a). This leakage dominates over the source-to-drain leakage current. Since the drain-to-bulk leakage current is gate bias independent, the drain leakage current is also insensitive to the gate bias.

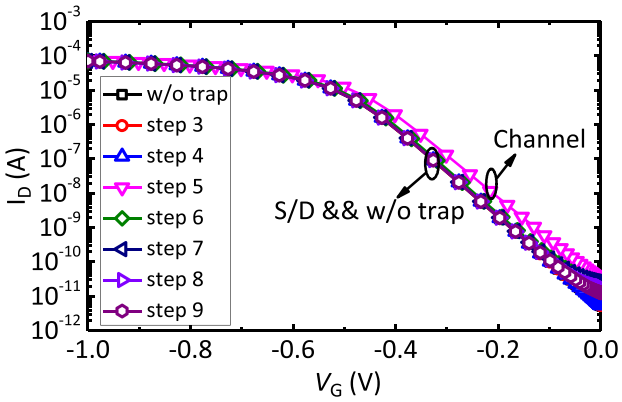

Fig. 3. Si pMOSFET drain current as a function of gate bias as the dislocation moves from source to drain. $V_D = -50$ mV.

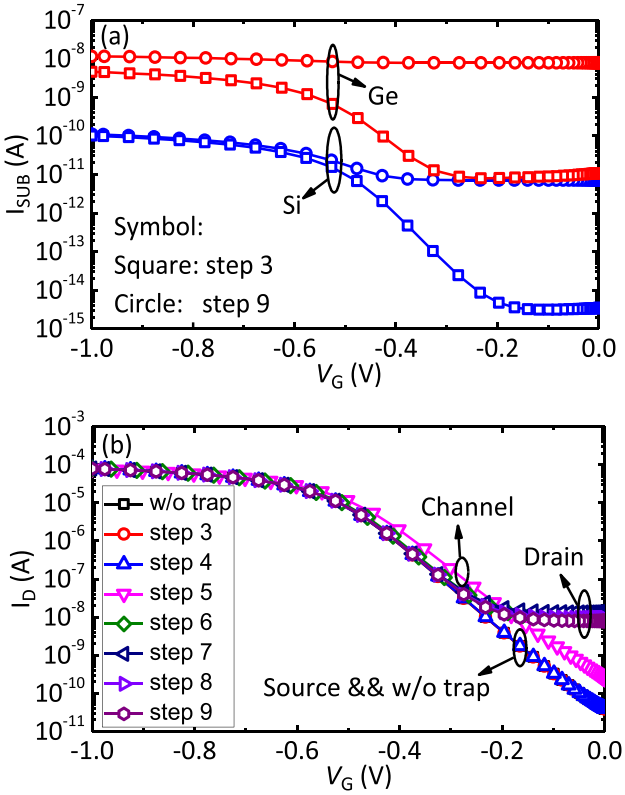

Fig. 4. (a) Substrate current for Si and Ge pMOSFET with dislocation at step 3 (in the source side) and step 9 (in the drain side). (b) Ge pMOSFET drain current with the dislocation at different positions. $V_D = -50$ mV.

The effect of a dislocation on the Ge pMOSFET characteristics, especially leakage current, strongly depends on the dislocation position in the device. Since epitaxially grown Ge on Si introduces TDs, this indicates that there should be a large variation of the device characteristics depending on the dislocation position in the device.

D. Discussion of 2-D Simulations

The simulations described earlier are 2-D rectangular based. For 2-D simulations in Sentaurus Device, the third dimension is effectively infinite [27], which makes the structure of Fig. 1 relevant to simulate wide, planar devices.

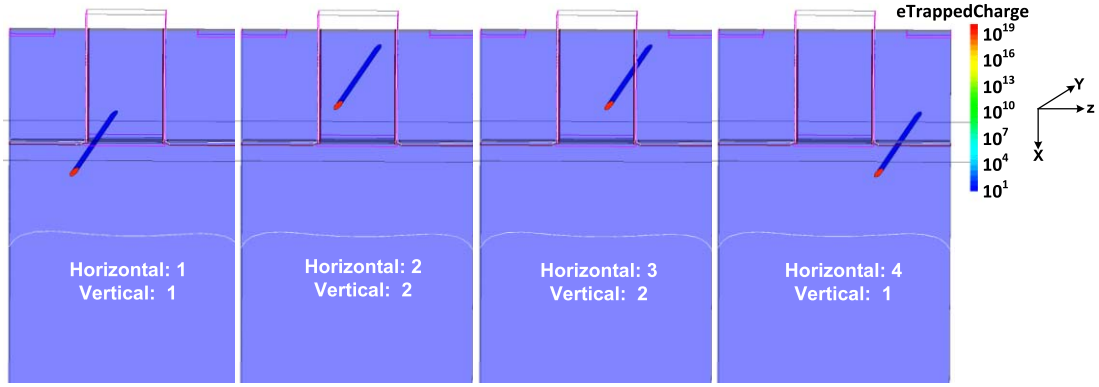

Fig. 5. Trapped electrons inside the dislocation with the dislocation at different locations in the device at $V_G = 0$ V, $V_D = 50$ mV, and $V_S = 0$ V. Horizontal 1–4 means the dislocation moves horizontally from source to drain and vertical 1–2 means that the dislocation moves vertically from below the active region to inside the active region. The FinFET size is $W_{\mathrm{FIN}} = 12$ nm, $H_{\mathrm{FIN}} = 35$ nm, and $L_G = 25$ nm.

In the simulation, the dislocation line shown in Fig. 1 is extended infinitely in the third direction. This corresponds to 2-D extended defects, such as stacking faults or twins. However, a dislocation in a real device has a small size in the third dimension, since it is a 1-D extended defect. Therefore, all the 2-D simulation results shown above correspond to planar defects in a real device. Nevertheless, the effect of a 1-D dislocation on transistor behavior may also be estimated from the 2-D simulation results.

Since the defective region extends in the third dimension on the order of $2r_{\mathrm{dis}}$ for a dislocation in a real transistor, a transistor with width W having a dislocation inside can be modeled as the parallel combination of a transistor with a 2-D planar defect having width $2r_{\mathrm{dis}}$ and a normal transistor without defect having width $W - 2r_{\mathrm{dis}}$. Therefore, the change of transistor characteristics due to a 1-D dislocation compared with a normal transistor without defect will be the 2-D simulation results, shown in Sections III-A–III-C, scaled by r_{dis}/W. For wide devices, the scaling factor is usually on the order of 1/100. So multiplying the 2-D simulation results by this scaling factor, it is likely that 1-D dislocations will have a negligible electrical effect on wide planar transistors. However, the effect will be more pronounced for narrower planar transistors.

E. Si FinFET

In this section, the effects of dislocations in n-channel Si FinFETs are considered using 3-D simulations. Fig. 5 shows a dislocation in four different locations in a Si FinFET device. Here, the $\langle 1\bar{1}0\rangle$ dislocation runs from the front surface to the back surface in the y-direction. The dislocation position is varied in the xz plane. In the z-direction, the dislocation moves from source to drain, and in the x-direction, it moves from below the active region to completely inside the active region.

Fig. 6(a) shows the device characteristics with the dislocation at different locations, as shown in Fig. 5. In contrast to the 2-D simulations, the transfer characteristic remains the same irrespective of the dislocation position. There is only a few millivolt threshold voltage shift. This is due to the well-controlled electrostatics by the gate in the FinFET [31]. The trapped electrons in the dislocation at $V_G = 0$ (OFF state), shown in Fig. 5, suggest that all the traps in the dislocation

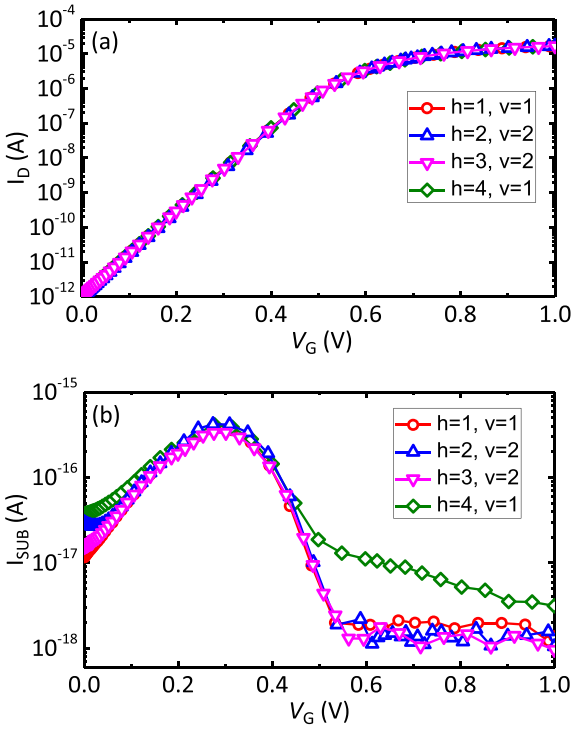

Fig. 6. Si FinFET (a) drain current and (b) substrate current as a function of gate bias with dislocation at different locations in the device. $V_D = -50$ mV. Here, h in the legend means horizontal and v means vertical, as shown in Fig. 5.

are filled in the OFF state. Though the gate voltage turns the device ON, it does not modulate the trap occupancy in the dislocation. As a result, the traps in the dislocation only contribute constant negative charges. Considering the small volume the dislocation occupies compared with the active region and high background doping (10^{18} cm^{-3}), the effect of this constant negative charge is negligible. Further simulation results confirm that the threshold voltage has a much more pronounced shift if the radius of the dislocation increases, since more trapped charges are contributed by the dislocation.

Fig. 6(b) shows the substrate current with the dislocation at different positions. The dislocation-induced leakage current is higher when the dislocation is in the drain substrate junction than all the other positions. This is consistent with the results obtained for the 2-D planar devices. This effect is not as

pronounced as in the 2-D planar devices, again due to the finite number of traps in the dislocation as represented in the simulations.

These results indicate that the electrostatic effect of a dislocation in a FinFET is negligible. However, since other mechanisms, such as dislocation-induced scattering, are not included in the present simulations and those mechanisms may be important in a confined structure, such as a FinFET [32], the total effect of dislocations in FinFETs requires further investigation.

IV. Conclusion

The electrical effects of single extended defects in MOSFETs are examined. The 2-D simulation results suggest that planar defects are a potential source of variability in planar transistors. The threshold voltage and SS increase only when the defect intersects the channel. The defect-induced leakage is the highest when the defect intersects the drain substrate junction. A simple scaling method has been applied to estimate the effect of a dislocation in a real transistor from the 2-D simulation results. The effect of a dislocation can be obtained from the 2-D simulation results scaled by the ratio between the dislocation radius and transistor width. The dislocation effect is more pronounced in narrow devices.

In addition, simulation results show that the dislocation has a small effect in FinFETs in terms of both threshold voltage shift and leakage current. This is due to the well-controlled electrostatics in FinFETs and the small number of defect states in the dislocation.

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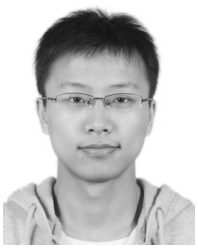

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